Development, Validation, and Application of Thermal Modeling for a MCM Power Package

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Abstract

This paper addresses the differences in thermal characterization and modeling for a multi-chip package with respect to a single-chip package. Since no thermal measurement system is commercially available to power more than one device during the test, the thermal model can be validated only with a single-heat source. Wires, which are used to connect the package under the test to the measurement system, should be included in thermal model to account for the heat sinking effect. The modeling results from the validated thermal model showed that the thermal behavior of a multi-chip package with a single heat-source does not truly represent the behavior in operating mode. The thermal resistance difference between the measured one from heating single device and that with three powered simultaneously might be as large as 100%. It is pointed out that the commonly adopted linear superposition method, which can be applied to thermal resistance characterization and measurement of components with multiple, independent heat sources within a package, might result in significant errors in a natural convection condition. A modified superposition method was developed in this paper, and has proved to be accurate to estimate the junction temperatures for a multi-chip module (MCM).

Keywords

Multi-chip module (MCM), junction temperature, thermal measurement, modeling, superposition

1 Introduction

The trend for new microprocessors is higher clock frequency to achieve faster processing. With each successive generation operating frequency, the performance and integration level have gone up, increasing power dissipation. At the same time, the operating voltage has gone down, thus driving up the current needed for given power level. As performance/frequency have increased, the required slew rates have gone up too. These demands add up to the requirement of higher power dissipation and lower parasitics for the design of voltage regulator module (VRM). The continuous reduction of the area of printed circuit board (PCB) also imposes challenges for the thermal design [1, 2].

The Philips Intelligent Power (PIP) device is a fully integrated solution for the output stage of a synchronous multi-phase buck regulator [3]. The devices consist of high side (control FET), low side (synchronous FET), and a FET driver (control IC). The PIP devices are designed to address the requirements of today's advanced microprocessors and high current DSP or ASIC devices. A split micro-leadframe (MLF^{TM}) package (see Fig. 1) allows the control FET, synchronous FET, and driver functions to be incorporated into a single package, lowering the parasitic impedances to minimize losses and optimize the performance. The integrated heat sinks that are embedded in the package provide the direct attachment of the heat sources to the PCB, thus greatly improving the thermal performance [2].

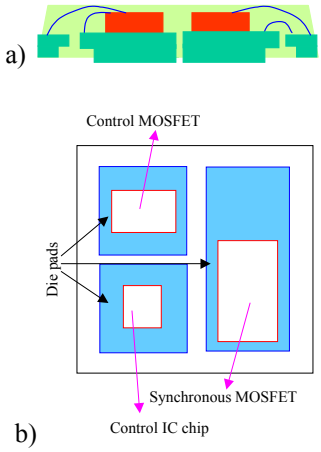

Fig. 1 A split micro-leadframe (MLF^{TM}) MCM package

Thermal characterizations of a split-leadframe multi-chip module (MCM) package are different from those of a single-chip package in various aspects. First, since no thermal measurement system is commercially available to power more than one device during the test, the thermal model can be validated only with a single-heat source. The validated thermal model can then be applied to investigate the thermal behavior in operating mode with all chips powering up. Second, it will be shown in this paper that the thermal behaviors of a multi-chip package with single-heat source mode do not truly represent the behaviors in operating mode with all chips powering up simultaneously. In order to obtain the junction temperatures in operating mode based on the single-heat source measurements, the common approach for a multiple-chip module is to use linear superposition [4]. This is true with the 'hard' boundary conditions [5], with which the non-linearity caused by the convection and radiation can be eliminated. However, there have been demands in predicting the junction temperatures precisely for a multiple-chip package in natural and forced convection conditions. This paper will present a modified superposition, with which the junction temperatures in operating mode with all chips powering up can be accurately estimated based on the single-heating mode results in convection conditions.

2 Validation of the Detailed Thermal Model for a Multi-Chip Micro-Leadframe Package

The measurement of junction temperatures was performed first for the MCM package shown in Fig. 1, with the thermal analyzer (e.g. ref. [4]). Due to the complexity of the inter-connections among three chips, cautions should be made to obtain the correct test data from the experiment. Our experiences indicated that, unless all pins of IC chip are shorted to ground for the package under study, the junction temperatures of synchronous MOSFET and control MOSFET chips, which are extracted from the forward voltage-drop with a small sense current, were almost 100% higher than when pins are all shorted to ground.

Table 1 lists the test results of the junction temperatures rise and thermal resistance, with heating the synchronous FET chip, for the package attached to the $1in^2$ 2 oz Cu on FR-4 board with the recommended layout [3], subject to the still air chamber. The results from Table 1 showed the repeatability of the test. It can be seen that the higher power level results in lower thermal resistance, because more turbulent airflow can be generated with higher power to dissipate relatively more heat away from the chip. The results also showed the differences of junction temperatures and thermal resistance between two MOSFETs when one of them is being heated. This indicated the effect of the split die-pads, by which the heat transferred from the heat source (heating chip) to another chip is not directly through the leadframe.

Table 1 Junction Temperature Measurement when Synchronous FET is powered up (FR-4 board, ambient: 24°C)*

Power (W)	Syn FET			Control FET		
	1st measurement	2nd measurement	Averaged Rja (C/W)	1st measurment	2nd measurement	Averaged Rja (C/W)
1.5	91.1	89.7	44.3	69.6	68.4	30.0
1.2	79.7	78.7	46.0	62.1	61.2	31.4
0.9	67.8	66.5	47.9	54.3	52.9	32.9
0.6	54.2	53.8	50.0	45.2	44.5	34.8
0.3	42.3	40.1	57.3	34.5	35.5	36.7
0.15	33.4	32.4	59.3	29.8	29.1	36.3

* Wires are included.

Let's now make comparisons of the modeling results with above test results. In order to accurately model the thermal environment of test system, the wires that connect the test samples to the adapter were taken into consideration, as shown in Fig. 2. CFD-based FLOTHERM™ software [6] has been used in this paper. Fig. 3 plotted both test and modeling results for heating Synchronous FET only. The numerical model predicts well the thermal behaviors with different power level and very good agreement with test was achieved.

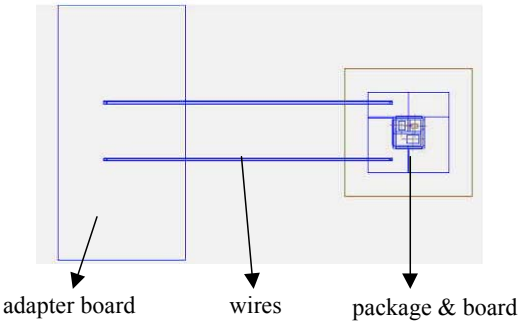

Fig. 2 Thermal model with wires and adapter board

Table 2 gives the results for the PIP package attached to an insulated metal substrate (IMS) board with a dimension of 61mmx34mm. Again the wires that connect the test sample to the adapter were included in our model. The calculated results agree well with the test results. The above results demonstrated that the detailed thermal model is reliable and consistent. We can use this model to investigate the thermal behaviors of this package in various powering modes, which can not be realized by the test.

Now let's investigate the impact of heat sinking through the wires that are used to connect the test sample to the system, but are not present in actual application. The diameter of each wire is 0.5mm. In Table 3, the validated thermal model is applied to obtain the junction temperatures and thermal resistances of three chips, which are tabulated with heating synchronous FET (1.5W) for both board attachments, FR-4 and IMS, respectively. It is surprising that the wires conduct about 36% heat in terms of thermal resistance, which corresponds to more than 25°C junction temperature difference (1.5W heat source and FR-4 board). The results show that the heat conducted through the wires is more significant for the package on 24mmx24mm FR-4 board than on 61mmx34mm IMS board. Since the capacity of heat dissipation through 24mmx24mm FR-4 board with one single copper layer on top is very limited, the wires connected to the copper area provide additional heat dissipation path to remove the heat. However, for the 61mmx34mm IMS board, the board area is relatively larger and the heat can be conducted throughout the board, thus the impact of the wires is not great.

Results in Table 3 indicated that the measurement of thermal resistance, i.e., R_{ja} with wires, or junction temperature, will not accurately represent the thermal resistance of package in actual use, in particular, when the package is attached to 24mmx24mm FR-4 board. The measured results have to be corrected through the simulation to obtain the R_{ja} without wires. For instance, the 'corrected' thermal resistance with powering synchronous FET only is about 65.9°C/W. This value is significantly higher than 44.3°C/W with wires (measurement in Table 1) or 49.7°C/W with wires by simulation.

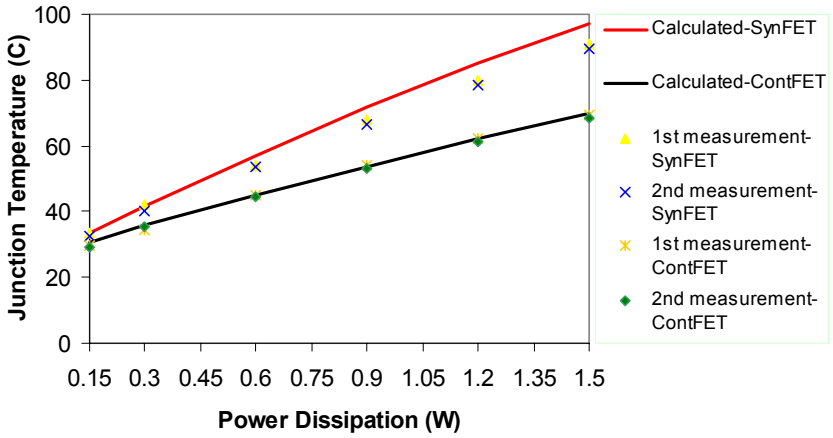

Fig. 3 Comparison of modeling and test results with only synchronous FET heating (Wires are included)

Table 2 Test and modeling results for PIP MLF package on IMS board (61mmx34mm) *

Junction temperature (C)	Powering SynFET				Powering ContFET			
	1.5W		2.0W		1.5W		2.0W	
	SynFET	ContFET	SynFET	ContFET	ContFET	SynFET	ContFET	SynFET
1st measurement	54.9	49.2	63.3	56.3	55	47.2	63.9	53.9
2nd measurement	56.2	50.4	65.2	57.7	57.2	49.8	66	56.6
Calculated	54.6	49.9	63.2	56.7	56.9	49.9	66.1	56.8

* Wires are included.

Table 3 Wire effects on the thermal behaviors during the test. (Values obtained using the thermal model)

Power mode	Powering Syn FET, 1.5W					
Board	24mmx24mm 2oz copper on FR-4			61mmx34mm IMS		
Junction	Syn FET	Cont FET	IC	Syn FET	Cont FET	IC
Tj without wires	122.8	95.1	91.1	58.1	53.3	53.5
Tj with wires	98.5	69.8	68.4	54.6	49.9	50.4
Rja without wires	65.9	47.4	44.7	22.7	19.5	19.7
Rja with wires	49.7	30.5	29.6	20.4	17.3	17.6
error in Tj	19.8%	26.6%	24.9%	6.0%	6.4%	5.8%
error in Rja	24.6%	35.6%	33.8%	10.3%	11.6%	10.5%

3 Thermal Behaviors of a Multi-Chip Package in Different Power Modes

Since the junction temperatures can be measured when one device only is powered up, the remaining question is how different the thermal resistance is with powering single device only from those with powering three simultaneously? To answer the question, the verified thermal model is applied with different powering modes. Assume that the total power loss on each PIP device is 3.0W. Four powering modes are considered. Power mode I, II, and III correspond to heating single synchronous FET, control FET and control IC, respectively. For power mode IV, the percentage of power dissipation on each chip is as following: 50% for synchronous FET, 33.3% for Control FET, and 16.7% for Control IC, which represents the typical operating condition for this PIP device [7]. When the total power dissipation is 3.0W, power mode IV is: 1.5W(synchronous FET)/1.0W(Control FET)/0.5W(Control IC). In the following the results will be presented based on the modeling results. Fig. 4 plotted the thermal resistance of each junction with respect to the ambient for 4 power modes respectively. We found that the thermal resistances with three chips powering simultaneously are very different from other three modes with single heat-source. Furthermore, the thermal resistances among three chips in a single-heat source are very different. It is inferred that the results of measurement by powering one device only will not truly represent the thermal behaviors of the package in actual operating mode. The thermal resistance difference between that obtained from heating single chip (e.g. heating IC) and that with three powering simultaneously can be as

large as nearly 100%. The reasons that cause such a difference can be two-fold. First, the heating source with a small area (one chip only) results in different junction temperatures from that with larger areas (e.g. three chips powered up at the same time). Second, the leadframe paddles beneath chips are separated, thus the heat can not be conducted directly from one chip to another chip through the leadframe and top-copper layer.

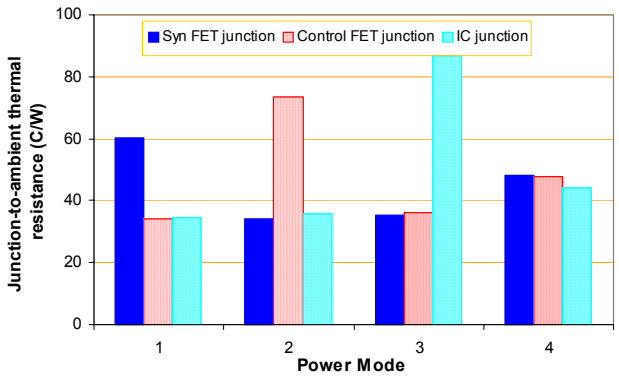

Fig. 4 Thermal behaviors of three chips in different powering modes for PIP MLF package
(Mode 1: Synchronous FET/Control FET/Control IC: 3.0W/0.0W/0.0W
Mode 2: Synchronous FET/Control FET/Control IC: 0.0W/3.0W/0.0W
Mode 3: Synchronous FET/Control FET/Control IC: 0.0W/0.0W/3.0W
Mode 4: Synchronous FET/Control FET/Control IC: 1.5W/1.0W/0.5W)

The above results are from the validated thermal model. An alternative approach is to use the linear superposition of measured values. The method of linear superposition may be applied to thermal resistance characterization and measurement of components with multiple, independent heat sources within a package [4]. Following single-source junction temperatures are measured,

ΔT_{11}: temperature rise of synchronous FET with aP W heating from synchronous FET

ΔT_{21}: temperature rise of control FET with aP W heating from synchronous FET

ΔT_{31}: temperature rise of driver IC chip with aP W heating from synchronous FET

ΔT_{12}: temperature rise of synchronous FET with bP W heating from control FET

ΔT_{22}: temperature rise of control FET with bP W heating from control FET

ΔT_{32}: temperature rise of driver IC chip with bP W heating from control FET

ΔT_{13}: temperature rise of synchronous FET with cP W heating from driver IC

ΔT_{23}: temperature rise of control FET with cP W heating from driver IC

ΔT_{33}: temperature rise of driver IC chip with cP W heating from driver IC

where P is the total amount of power dissipation for three chips, a, b and c are the percentage ratio of power dissipation by three chips respectively, and $a+b+c=1$. ΔT_{ij} (i,j = 1,2,3), the junction temperature rise matrix, can be obtained from the measurement. The junction temperatures with heating from three chips simultaneously, i.e., aP W(synchronous FET)/bP W(control FET)/cP W(driver IC), can then determined by linear superposition:

$$\begin{aligned}\Delta T_1&=\Delta T_{11}+\Delta T_{12}+\Delta T_{13}\\ \Delta T_2&=\Delta T_{21}+\Delta T_{22}+\Delta T_{23}\\ \Delta T_3&=\Delta T_{31}+\Delta T_{32}+\Delta T_{33}\end{aligned} \quad (1)$$

where the ΔT_1, ΔT_2 and ΔT_3 are the junction temperature rises for synchronous FET, control FET and driver IC, respectively, with powering three simultaneously.

Let's use the above equations to check the validity of the linear superposition. With the help of the simulation, ΔT_{ij} (i,j = 1,2,3) can be calculated with a=50%, b=33.3% and c=16.7%[7]. In Fig. 5, the results from the linear superposition based on equation (1) were compared to the results with mode 4 in Fig. 4. It clearly showed that the errors from the linear superposition are as large as 17%, which correspond to the temperature difference of 24C° when the total power dissipation is 3.0W. This is because the system involved with the airflow and the radiation effect is non-linear.

The linear superposition works well for a linear system with 'hard' boundary conditions [5]. However, often the thermal test is performed under natural or forced convection conditions, in which the non-linearity is inevitable. In the following section, a modified superposition will be proposed to account for the non-linearity of system.

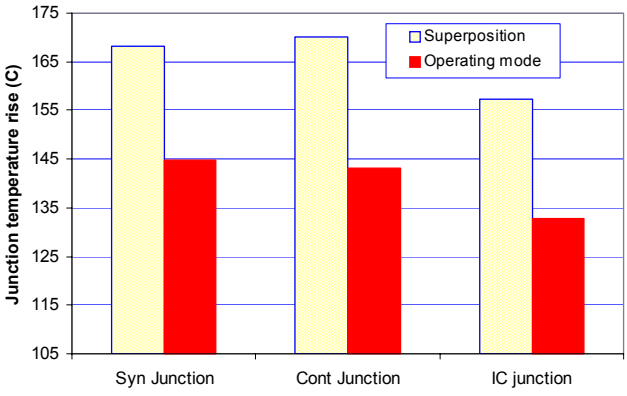

Fig. 5 Comparison of linear superposition with results in operating mode
(power dissipation 3W, 1in^2 FR-4 with single layer Cu)

4 Accurate Estimate of Junction Temperatures for Multi-Chip Package – Modified Superposition Method

Let's look at the governing equations of the system with the fluid flow and radiation, which can be written as following,

The conservation of mass

$$\frac{\partial \rho}{\partial t}+\frac{\partial}{\partial x_i}(\rho u_i)=0 \tag{2}$$

The conservation of momentum

$$\frac{\partial}{\partial t}(\rho u_j)+\frac{\partial}{\partial x_i}(\rho u_i u_j)=\frac{\partial}{\partial x_i}(\mu\frac{\partial u_j}{\partial x_i})-\frac{\partial p}{\partial x_j}+S_j \tag{3}$$

and, the conservation of energy

$$\frac{\partial}{\partial t}(\rho c_p T)+\frac{\partial}{\partial x_i}(\rho u_i T)=\frac{\partial}{\partial x_i}(k\frac{\partial T}{\partial x_i})+P \tag{4}$$

where ρ is the density; u_i the velocity vector (i=1,2, and 3), p the pressure, T the temperature, S_j the body force, P the heat source, and μ is viscosity. The nonlinear effect of radiation can be written as

$$-q=\alpha(T^4-T_0^4) \tag{5}$$

where α is the coefficient of radiation and q is the heat flux through the radiation area, and T_0 is the ambient temperature.

Let's now confine our attention to the heat transfer through the solid part of the system, i.e., the interior package. In this case, if we assume that the thermal properties of package materials are linear, the governing equation can be re-written as following

$$\rho c_p\frac{\partial T}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial T}{\partial x_i})+P(X) \tag{6}$$

with the following boundary conditions

$$-k\frac{\partial T}{\partial n}=h(T-T_0)+\alpha(T^4-T_0^4) \tag{7}$$

where T the temperature on the boundary , h is the heat transfer coefficient that is dependant on T and air flow , k the thermal conductivity, and n the normal of the surface. It can be seen that all non-linearity of the system appears at the solid/fluid boundary. This makes the problem simpler since the heat conduction inside is linear. When three chips generate heat simultaneously in operating mode, the heat source in equation (6) can be expressed as

$$P(X)=P\cdot[a\delta(X_1)+b\delta(X_2)+c\delta(X_3)] \tag{8}$$

where P is the total amount of heat dissipation, a, b and c are the percentage ratios of power generation for synchronous FET, control FET and driver IC respectively. X_1, X_2 and X_3 mean the location of heat sources. Thus equation (6) can be re-written as

$$\rho c_p\frac{\partial T}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial T}{\partial x_i})+P\cdot[a\delta(X_1)+b\delta(X_2)+c\delta(X_3)] \tag{9}$$

For the single heating-source modes, assuming that the power level remains same as that with powering three chips simultaneously, the governing equations can be written as following, respectively,

Powering synchronous FET with the total amount of P

$$\rho c_p\frac{\partial T^{(1)}}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial T^{(1)}}{\partial x_i})+P\delta(X_1) \tag{10}$$

Powering control FET with the total amount of P

$$\rho c_p\frac{\partial T^{(2)}}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial T^{(2)}}{\partial x_i})+P\delta(X_2) \tag{11}$$

Powering control IC with the total amount of P

$$\rho c_p\frac{\partial T^{(3)}}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial T^{(3)}}{\partial x_i})+P\delta(X_3) \tag{12}$$

where $T^{(1)}$, $T^{(2)}$ and $T^{(3)}$ are the temperature fields with heating single synchronous FET, control FET and driver IC respectively. Since the power magnitude is same as that when three chips are powered on, it is expected that the airflow caused by such a power is similar and the temperature on the majority of the solid boundaries including the attached board is same. With this assumption, the above three cases share the same boundary conditions with same h, T and T_0 by equation (7).

Now let's multiply a, b and c to equations (10), (11) and (12) respectively, with the boundary conditions, as following

$$\rho c_p\frac{\partial aT^{(1)}}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial aT^{(1)}}{\partial x_i})+aP\delta(X_1) \text{ with}$$

$$-ak\frac{\partial T}{\partial n}=ah(T-T_0)+a\alpha(T^4-T_0^4) \tag{13}$$

$$\rho c_p\frac{\partial bT^{(2)}}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial bT^{(2)}}{\partial x_i})+bP\delta(X_2) \text{ with}$$

$$-bk\frac{\partial T}{\partial n}=bh(T-T_0)+b\alpha(T^4-T_0^4) \tag{14}$$

$$\rho c_p\frac{\partial cT^{(3)}}{\partial t}=k\frac{\partial}{\partial x_i}(\frac{\partial cT^{(3)}}{\partial x_i})+cP\delta(X_3) \text{ with} \tag{15}$$

$$-ck\frac{\partial T}{\partial n}=ch(T-T_0)+c\alpha(T^4-T_0^4)$$

Summing up equations (13), (14) and (15), we obtain

$$\rho c_p\frac{\partial(aT^{(1)}+bT^{(2)}+cT^{(3)})}{\partial t}=k\frac{\partial}{\partial x_i}[\frac{\partial(aT^{(1)}+bT^{(2)}+cT^{(3)})}{\partial x_i}]$$
$$+P\cdot[a\delta(X_1)+b\delta(X_2)+c\delta(X_3)]$$

with (16)

$$-(a+b+c)k\frac{\partial T}{\partial n}=(a+b+c)h(T-T_0)$$
$$+(a+b+c)\alpha(T^4-T_0^4) \tag{17}$$

Since $a+b+c=1$, and let

$$T=aT^{(1)}+bT^{(2)}+cT^{(3)} \tag{18}$$

Equation (16) becomes exactly same as the equation (9) that we try to solve. This implies that the solution of equation (9) can be obtained from equation (18) when $T^{(1)}$, $T^{(2)}$ and $T^{(3)}$ are known. Therefore the three junction temperatures can now be expressed as according to equation (18)

$$\Delta T_1=a\Delta T_{11}+b\Delta T_{12}+c\Delta T_{13}$$
$$\Delta T_2=a\Delta T_{21}+b\Delta T_{22}+c\Delta T_{23} \tag{19}$$
$$\Delta T_3=a\Delta T_{31}+b\Delta T_{32}+c\Delta T_{33}$$

Equation (19) is different from the traditional linear superposition, expressed by equation (1). The single-source temperatures ΔT_{ij} are defined differently, as following

ΔT_{11}: temperature rise of synchronous FET with P W heating from synchronous FET

ΔT_{21}: temperature rise of control FET with P W heating from synchronous FET

ΔT_{31}: temperature rise of driver IC chip with P W heating from synchronous FET

ΔT_{12}: temperature rise of synchronous FET with P W heating from control FET

ΔT_{22}: temperature rise of control FET with P W heating from control FET

ΔT_{32}: temperature rise of driver IC chip with P W heating from control FET

ΔT_{13}: temperature rise of synchronous FET with P W heating from driver IC

ΔT_{23}: temperature rise of control FET with P W heating from driver IC

ΔT_{33}: temperature rise of driver IC chip with P W heating from driver IC

which are obtained from the measurement with maintaining the same power level as the total power of three chips. And then, the percentage ratios a, b and c will be multiplied in equation (19). In Fig. 6, the results from the modified superposition based on equation (19) were compared to the results with actual operating mode. It clearly shows that the error is controlled well within 2%, compared to the 17% previously. This means that maintaining the same power level for different powering modes affect the temperature distributions inside the package greatly, but have little influences on the boundary temperatures and environmental conditions, excepting to the zone on the boundary that is very close to the heat sources.

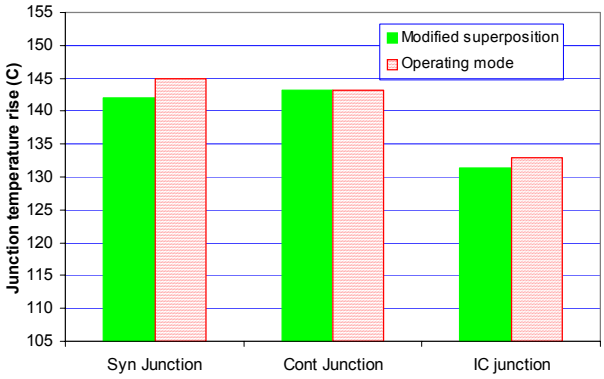

Fig. 6 Comparison of the modified superposition with results in operating mode
(power dissipation 3W, 1in^2 FR-4 with single layer Cu)

Let's now consider the forced convection condition. In Fig. 7, the results from the direct superposition and the modified superposition are compared to the results in operating mode, with the airflow rate of 100 LFM. Under the forced convection condition, the heat transfer coefficient on the surface is more dominated by the external airflow rate, rather than the self-heating effect from the package. Therefore, the direct superposition approach presents better results than it does under natural convection condition. Nevertheless, the modified superposition gives more accurate predictions of the results.

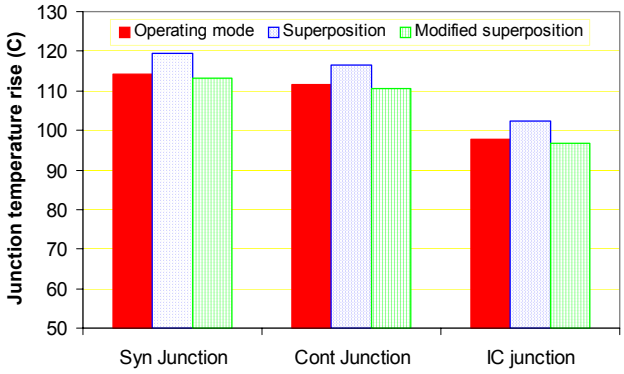

Fig. 7 Comparisons of different superposition methods in forced convection condition
(power dissipation 3W, 1in^2 FR-4 with single layer Cu)

5 Conclusion

A detailed thermal model has been developed for a multi-chip MLF package with split die-paddles. The model has been validated against the junction temperature measurement. However, due to the fact that the thermal test system is not able to power more than one device simultaneously, the validated model should be applied to obtain the thermal behavior in operating mode. It was shown that the thermal behavior of a multi-chip package with a single heating-source is not validly extended to describe multiple-chip package. The thermal resistance difference between the measured one from heating single chip and that with three powering simultaneously might be as large as 100%. This is because the heat can not be conducted directly from one chip to another by the separated die pads.

A modified superposition has been developed in this paper and applied to the thermal resistance characterization and measurement of components with multiple, independent heat sources. The idea behind this method is to maintain the heating power level as same as the total power when single-chip is heated up. The non-linearity caused by the convection and radiation can then be eliminated. It has been shown that the error of the junction temperatures in the operating mode by the modified superposition can be controlled within 2%, while the original linear superposition gives the error as large as 20%.

References

1. Sawle, Andrew, Blake, Carl, & Mariae, Dragan, "Novel Power MOSFET Packaging Technology Doubles Power Density in Synchronous Buck Converter for Next Generation Microprocessors", *APEC*, pp. 106-111, 2002.
2. Fan, Xuejun & Haque, S., "Emerging MOSFET Packaging Technologies and Their Thermal Evaluation", Proc. Of 8th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM 2002, pp. 1102-1108, 2002.

3. Philips Semiconductors, PIP201-12M: DC to DC converter powertrain: preliminary data sheet*, Rev. 01-23*, January 2002.
4. Sofia, John, "Fundamentals of Thermal Resistance Testing", http://www.analysistech.com.
5. Lasance, Clemens, J. M., Rosten, Hervey, I., & Parry, John, D. Parry, "The World of Thermal Characterization According to DELPHI – Part II: Experimental and Numerical Methods"*, IEEE Transactions CPMT*, 20(4), 392-398, 1997.
6. FLOMERICS, FLOTHERM 3.2, 2002.
7. Rutter, P., & Kanwar, K., "Motherboard VRM Power Loss Analysis", Philips Semiconductors Internal Report, June 2001.